§102 Rejection of the Claims

Claims 10, 11, 13, 14, 17, 18, 20, 23, 24, 29, 33-38, 44, and 45 were rejected under 35 USC § 102(e) as being anticipated by Austin (U.S. 5,982,690). Applicant respectfully traverses these grounds for rejection for the reasons argued below.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that the Austin patent is distinguishable from the present invention.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation because Austin does not teach or suggest each and every element of applicant's claims arranged as in the claims.

Claim 10 recites: "a dual-gated metal-oxide semiconducting field effect transistor." In contrast, Austin merely describes "third and fourth parallel connected (PC) transistor pairs 153 and 154." *Austin at column 5, lines 7-10 and Fig. 1D.*

Applicant respectfully submits that the Austin "third and fourth parallel connected (PC) transistor pairs 153 and 154" does not teach or suggest a "a dual-gated metal-oxide semiconducting field effect transistor" as required by claim 10 because a parallel connected transistor pair consists of two transistor devices in parallel, while a dual-gated metal-oxide semiconducting field effect transistor is one device having two gates. Applicant notes on page 10, lines 22-24 of the specification that a dual-gated metal-oxide semiconducting field effect transistor will divide the metal-oxide semiconducting field effect transistor into two transistors when the dual gates are in parallel. However, the dual-gated metal-oxide semiconducting field

effect transistor is a specific device that is distinct from the Austin "transistor pairs 153 and 154." Austin does not specifically teach or suggest the specific device, namely "a dual-gated metal-oxide semiconducting field effect transistor."

The Office Action states:

> Applicant does not provide any prior art that teaches the claimed dual-gated MOSFET transistor to show the structure of the dual-gated transistor as shown in the drawing is well known. As best understood by the drawing, a dual-gated MOSFET transistor comprises two MOS transistors connected in parallel. Austin's figure 1D shows a circuit (e.g. 127) comprises two MOS transistor transistors connected in parallel. Therefore, circuit 127 can be considered as a dual-gated MOSFET transistor.

Applicant traverses this statement for several reasons. The expression "a dual-gated MOSFET transistor" has several components. The term "transistor"is the primary subject where the terms "a", "dual-gated", and "MOSFET" modify the term "transistor". The term "transistor" is well known to have several versions. One version of "a" "transistor" is "a MOSFET transistor," where "a MOSFET transistor" implies a single structure. "A MOSFET transistor" is known to have a drain, a source, and a gate. The term "dual-gate" modifies the known "a MOSFET transistor" in a specific manner, that is, the known "a MOSFET transistor" is modified to have two gates for the single structure. However, the two gates can be in series or in parallel. Though the original specification on pages 9-10 discloses that the two gates of the dual-gated metal-oxide semiconducting field effect transistor are in parallel, Fig. 2A was previously amended to reference the disclosure in the specification.

In the specification on page 10 line 17-18, a dual-gated metal oxide effect transistor is now referenced as item 298 in Fig. 2A (a second dual-gated metal oxide effect transistor is referenced as Item 299 in Fig. 2A), which in the figure clearly indicates that Applicant's disclosed dual-gated metal oxide effect transistor has two gates in parallel, as disclosed in the written description of the original specification. Upon reading the specification page 10 and Fig.

2A, the structure of Applicant's invention including use of dual-gated metal oxide effect transistors can be understood, though there is not a standard drawing symbol for a dual-gated metal oxide effect transistor.

Additionally, Fig. 2A can be compared with Fig. 4, where the symbols for M3 and M5 (also, M4 and M6) show M3 and M5 as two transistors in parallel for the memory device disclosed in Fig. 4. Clearly, the transistors M3 and M5 as shown in Fig. 4 use standard transistor device symbols joined together in parallel at two nodes, one node coupled to V1 and the other node coupled to node 7. One node is also coupled to the M3 drain and to the M4 drain, and the other node is also coupled to the M3 source and to the M4 source. As shown in Fig. 4, the drains and sources for M3 and M5 are separately distinct (also M4 and M6). Thus, since the symbols used in Fig. 2A and Fig. 4 are different, and Fig. 4 uses standard symbols, Fig. 4 demonstrates that the symbols for M3, M5 and M4, M6 used in Fig. 2A cannot be taken as limiting M3,M5 and M4,M6 to two distinct transistors in parallel.

Further, as demonstrated above, the plain meaning of a dual-gated metal oxide field effect transistor as used in claim 10 is a single MOSFET having one drain, one source, and two gates. References were identified in the previous response to the Office Action mailed on 18 July 2001 [Denton, J.P. et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate," IEEE Electron Device Letters, 17(11),509-511,(Nov.1996), Mizumo, T. et al., "High Performance Characteristics in Trench Dual-Gate MOSFET (TDMOS)," IEEE Transactions on Electron Devices, 138(9),2121-2127,(Sept.1991), and Frank, D.J. et al., "Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?," IEDM TECHNICAL DIGEST: INTERNATIONAL ELECTRON DEVICES MEETING, 21.1.1-21.1.4, (Dec.1992)] that demonstrated that Applicant's use of the term dual-gated metal oxide field effect transistor is an appropriate term that can be understood by those skilled in the art by reading the specification. Since there is no standard symbol for a dual-gated metal oxide field effect transistor for use in a circuit, the parallel combination of M3 and M5 are enclosed in the dashed lines labeled 298 which references M3 and M5 to the specification where they are disclosed as a single dual-gated metal oxide field effect transistor (similarly, for M4 and M6 with respect to label 299). Since 298 is

part of Fig. 2A the specification must be referenced when determining meaning in the figure. Referring to the written description for label 298, the drawing including 298 indicates use of a dual-gated metal oxide semiconductor field effect transistor as recited in the claims. If the drawing were to be considered separate from the specification there would be no need for any labeling, but such labeling is required. The figures and the specification are part and parcel of the patent application. Therefore, given the written description in the specification, a dual-gated metal oxide field effect transistor can not be understood to be two distinct MOS transistors connected in parallel.

To apply the broadest reasonable interpretation to a claim, the meaning applied to terms in the claim, such as "a dual-gated metal oxide transistor," must be consistent with the specification. According to M.P.E.P. § 2111 discussing *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997):

> The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the 'PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification.' (underlining added)

Applicant's specification page 9 lines 25-25 discloses an inverter B1 shown in Figure 2A having a pair of transistors M3, M5 (M3 and M5 are shown in Figure 2A as parallel). In contrast, Application's specification page 10 lines 16-18 discloses an alternate embodiment where M3 and M5 comprise a dual-gated metal oxide semiconductor field effect transistor, now labeled 298. Applicant clearly and specifically defines a dual-gated metal oxide semiconductor field effect transistor as being different, or alternate, to a pair of transistors. In light of the references stated above and identified in a previous response to an Office Action, one of ordinary skill in the

art upon reading the written description of the specification would clearly follow the applicant's disclosure and defining description that a dual-gated metal oxide semiconductor field effect transistor is not a pair of transistors, but an alternate device.

Further, Austin specifically recites "third and fourth parallel connected (PC) transistor pairs 153 and 154", clearly indicating two distinct transistors in each pair. There is no suggestion or teaching about a specific transistor such as a dual-gated metal oxide field effect transistor, either in Austin's drawing or specification. Therefore, the "circuit" 127 can not be considered as a dual-gated MOSFET transistor, as required by claim 10. Thus, Applicant respectfully submits that Austin does not teach or suggest all the elements of claim 10, as recited in the claim.

Independent claims 17, 23, 29, 32, 33, 37, 40, 44, and 45 recite similar elements as claim 10 and are patentable over Austin for similar reasons as those argued above, plus the elements in the claims. Claims 11, 13, and 14 depend from claim 10, claims 18 and 20 depend from claim 17, claims 24 depends from claim 23, claims 34-36 depend from claim 33, and claim 38 depends on claim 37 and are patentable over Austin for the reasons argued above, plus the elements in the claims.

Applicant respectfully requests withdrawal of the rejection of claims 10, 11, 13, 14, 17, 18, 20, 23, 24, 29, 33-38, 44 and 45 under 35 USC § 102(e), and reconsideration and allowance of these claims.

§103 Rejection of the Claims

Claims 15, 16, 21, 22, 26, 27, and 30-32 were rejected under 35 USC § 103(a) as being unpatentable over Austin (U.S. 5,982,690).

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that the Austin patent is distinguishable from the present invention.

The Examiner rejected claims 15, 16, 21, 22, 26, 27, and 30-32 based on Austin. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found Austin. Since all the elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the

missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

As to claims 15, 16, 21, 22, 26, 27, and 30-32, these claims cite using a dual-gated metal oxide semiconductor. In contrast, Austin in Fig. 1D and col.5 lines 7-10 cites " third and fourth parallel connected (PC) transistor pairs 153 and 154." Nowhere does Austin disclose, teach or suggest the use of a dual-gated transistor in a latch, amplifier, or sense amplifier. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02. Since Austin does not disclose, teach, or suggest every element of these claims, claims 15, 16, 21, 22, 26, 27, and 30-32 are patentable over Austin.

Applicant respectfully requests withdrawal of the rejection of claims 15, 16, 21, 22, 26, 27, and 30-32 under 35 USC § 103(a), and reconsideration and allowance of these claims.

Claims 28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (U.S. 6,069,828) in view of Austin (U.S. 5,982,690).

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that the Austin patent is distinguishable from the present invention.

As to claims 28 and 40-43, these claims cite using a dual-gated metal-oxide semiconductor. As mentioned above, Austin does not disclose, teach, or suggest the use of a

dual-gated transistor. As to Kaneko et al., the Office Action states in reference to Kaneko et al. that "figure 2 shows all the elements of the claim except for the detail of the sense amplifier," indicating that Kaneko et al. nowhere discloses, teaches, or suggests a dual-gated transistor. Since neither Austin, Kaneko et al. or their combination disclose, teach, or suggest all the elements of these claims, claims 28 and 40-43 are patentable over Kaneko et al. in view of Austin.

Applicant respectfully requests withdrawal of the rejection of claims 28 and 40-43 under 35 USC § 103(a), and reconsideration and allowance of these claims.

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612 371-2157) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Amy Moriarty
Amy J. Moriarty

Feb. 4, 2002
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